An 8V Organic Complementary Logic Process for Flexible Polymeric Substrates

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We have designed and fabricated the first organic complementary integrated circuits on a flexible substrate. Pentacene and hexadecafluorocopperphthalocyanine ($F_{16}CuPc$) were used as the p-type and n-type organic semiconductors, and solution-processed polyvinylphenol was used as the gate dielectric. Transistors and circuits operate with a supply voltage as low as 8 V, and ring oscillators have a signal propagation delay as low as 8 µsec per stage. To our knowledge, these are the fastest organic complementary circuits reported to date.

In principle, complementary circuits have several advantages over integrated circuits based on a single carrier type, including lower power dissipation, greater speed, and better noise margins. The problem with organic complementary circuits is the small electron mobility of even the best air-stable organic semiconductors. The Philips group has reported ambipolar TFTs and inverters based on narrow-bandgap polymers and interpenetrating networks of p-type and n-type materials, but the electron mobilities in these materials are below 10^{-4} cm^2/Vs, even when the devices are measured in vacuum [1]. Crone and coworkers have demonstrated organic TFTs based on sexithiophene (with a hole mobility of 0.016 cm^2/Vs) and $F_{16}CuPc$ (with an electron mobility of 0.02 cm^2/Vs) and reported complementary circuits with a signal propagation delay of 10 µsec per stage. These circuits were fabricated on silicon wafers with inorganic gate dielectrics and were operated in ambient air with a supply voltage of 100 V [2].

We have recently developed a manufacturing process for organic TFTs on flexible polymeric substrates, using a solution-processed polyvinylphenol (PVP) gate dielectric layer [3]. To scale supply voltage and circuit performance, the PVP thickness can be reduced to less than 100 nm without introducing prohibitive gate leakage. Figure 1 shows that the current density through an 80 nm thick PVP layer is 0.5 $\mu A/cm^2$ at a gate voltage of 8 V and 1 mA/cm^2 at 25 V. Also shown in Figure 1 are the electrical characteristics of a pentacene TFT fabricated on 125 µm thick, flexible polyethylene naphthalate (Teonex® Q65 PEN, provided by DuPont Teijin Films, Wilton, U.K.), with an Al gate electrode, a 50 nm thick PVP gate dielectric, Au source/drain contacts, and evaporated pentacene, and with a hole mobility of 0.1 cm^2/Vs and a subthreshold swing of 0.6 V/decade. Figure 2 shows the characteristics of a polymer-gate-dielectric $F_{16}CuPc$ TFT, with an electron mobility of 0.002 cm^2/Vs and a subthreshold swing of 1.4 V/decade. Although the mobility of these $F_{16}CuPc$ TFTs is smaller than the mobility of most p-channel organic TFTs, it is to our knowledge the best performance reported for an n-channel organic TFT on a flexible substrate. All electrical measurements reported here were performed in air under ambient conditions.

The schematic cross section of our complementary circuits is shown in Figure 3. After defining the Al gate electrodes, the PVP gate dielectric layer (with vias for interconnects), and the Au source/drain contacts, the pentacene active layer is deposited and patterned using a water-soluble photoresist and a brief O_2 plasma etch [4]. This is followed by the deposition of the $F_{16}CuPc$ active layer, which is not patterned, since we found that the described resist process leads to an unacceptable degradation of the $F_{16}CuPc$ mobility. By adjusting the W/L ratios of the p-channel and n-channel TFTs to account for the difference in mobility, complementary inverters with sufficiently large gain are obtained (see Figure 3).

The chip micrograph in Figure 4 shows that by lithographically patterning at least one of the two organic semiconductors, the density of the circuit layout can be significantly increased compared with the approach described by Crone et al. who used shadow masks to pattern the semiconductors [2]. A 5-stage ring oscillator like the one shown in Figure 4 occupies an area of less than 0.5 mm^2. Also shown in Figure 4 is the signal propagation delay measured for 5-stage complementary ring oscillators as a function of design rule and supply voltage. The circuits operate with a supply voltage as low as 8 V and with a signal delay as low as 8 µsec per stage (using a design rule of 2 µm and a supply voltage of 40 V). To our knowledge, these are the fastest organic complementary circuits reported to date, and the first on a flexible substrate.

[1] E. J. Meijer et al., *Nature Materials*, vol. 2, p. 678 (2003)
[2] B. Crone et al., *Nature*, vol. 403, p. 521 (2000); *J. Appl. Phys*. vol. 89, p. 5125 (2001)
[3] H. Klauk et al., *Appl. Phys. Lett.*, vol. 82, p. 4175 (2003)
[4] C. D. Sheraw et al., *Appl. Phys. Lett.*, vol. 80, p. 1088 (2002)

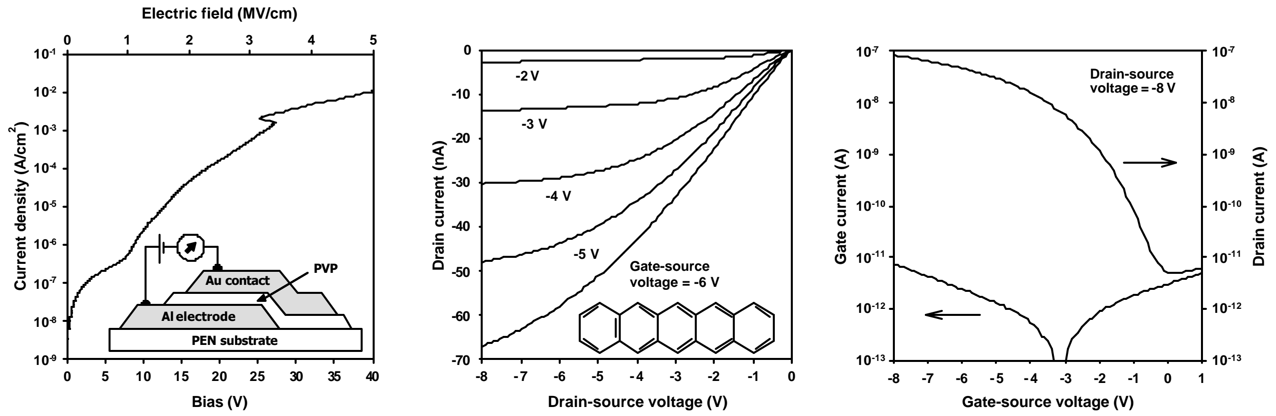
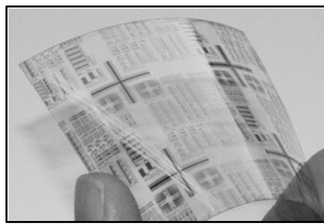


Fig. 1. Leakage through an 80 nm thick polyvinylphenol (PVP) gate dielectric layer, and electrical characteristics of a pentacene TFT on PEN after patterning the pentacene active layer as shown in Figure 3. The pentacene TFT has a W/L ratio of 1.



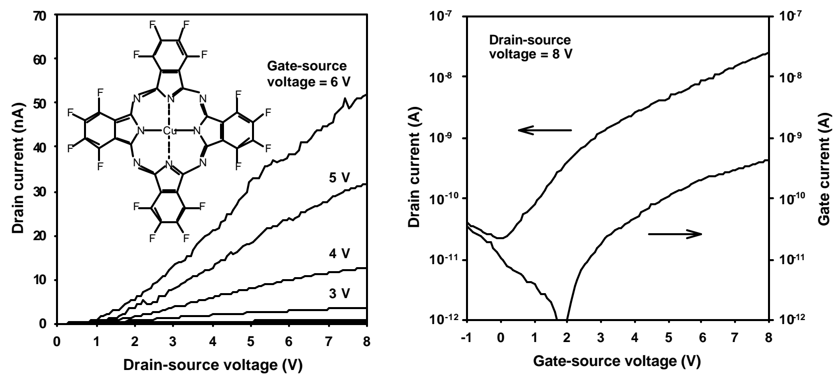
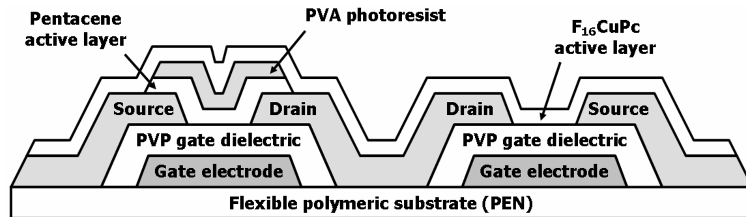


Fig. 2. Photograph of a flexible PEN test chip, and electrical characteristics of a $F_{16}CuPc$ TFT. The $F_{16}CuPc$ TFT has a W/L ratio of 25.



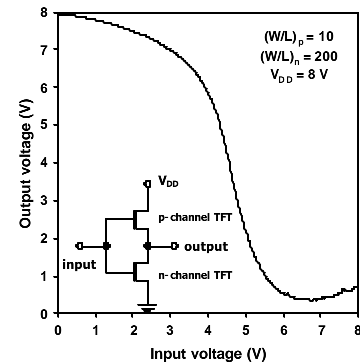
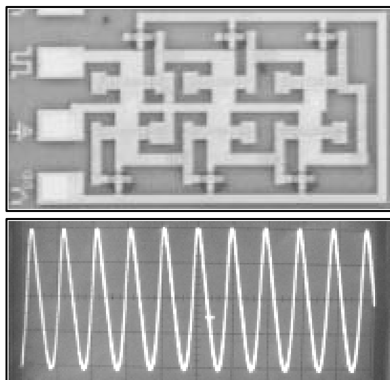


Fig. 3. Schematic cross section and static transfer characteristics of a complementary organic inverter. At a supply voltage of 8 V, the inverter has a small-signal gain of 6.



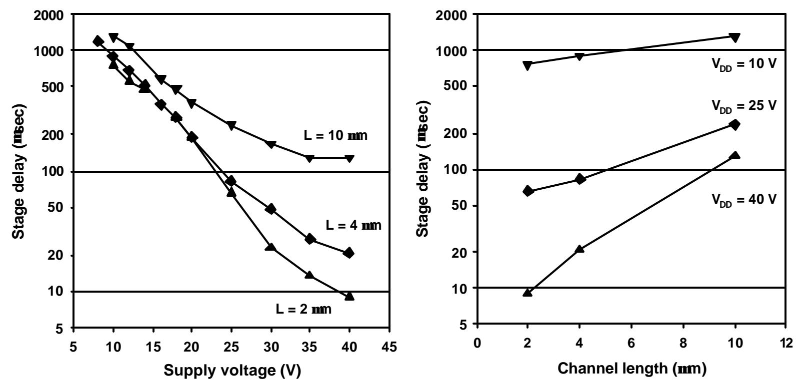


Fig. 4. Optical micrograph and output signal of a 5-stage complementary ring oscillator on flexible PEN, and signal delay measured for ring oscillators based on three different design rules as a function of supply voltage and channel length.

Collector Vertical Scaling and Performance Tradeoffs in 300 GHz SiGe HBTs

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With its operation speed penetrating into 300 GHz regime [1], SiGe HBT (Heterojunction Bipolar Transistor) emerges as a viable technology option for millimeter-wave applications, such as 60 GHz broadband WLANs (Wireless Local Area Networks), 77 GHz automotive radars, etc. The principal device design strategy for the rapid speed enhancement has been the continuous vertical scaling, which proved highly effective, especially for the cutoff frequency f_T improvement. However, such vertical scaling inevitably involves increases in the base-collector junction capacitance (C_{CB}) as well as the base resistance (R_B), which have adverse effects on the maximum oscillation frequency f_{max}. This study investigates the impact of the collector vertical scaling on such tradeoff between f_T and f_{max}, with SiGe HBTs of ~300 GHz performance. We further proceed to discuss its impact on the avalanche breakdown behavior of the devices.

The schematic cross section of a typical SiGe HBT used for this study is shown in Fig. 1, which is based on the double-poly structure with a UHVCVD-grown SiGe base layer (see [2] for detailed device structure description). Fig. 2 and Fig. 3 present the DC and RF characteristics, respectively, of the control device. The maximum current gain is ~650, with the base and the collector ideality factors extracted to be 1.08 and 1.03, respectively. BV_{CEO} is 1.6 V while BV_{CBO} is 5.4 V. f_T and f_{max}, extracted from the extrapolation of h_{21} and U at 40 GHz with –20 dB/dec roll-off assumption, exhibit peak values of 310 GHz and 295 GHz, respectively.

One of the most widely employed techniques for collector vertical scaling in Si-based bipolar transistors is to control the ion implant dose of SIC (Selectively Implanted Collector). In this work, three different SIC conditions were implemented and corresponding device characteristics were compared. SIC_H represents the control device, while SIC_M and SIC_L represent devices with reduced SIC doses: ~50 % and ~30 % of the total integrated dose of SIC_H, respectively. As Fig. 4 and Fig. 5 indicate, f_T is degraded as SIC dose decreases. This is due to the increased B-C space charge region (SCR) width (Fig. 6) that leads to an increase in the B-C SCR transit time. The increased B-C SCR width, on the other hand, accompanies a reduction in C_{CB} (Fig. 6). The net effect is an enhancement in f_{max}, which is roughly expressed by $(f_T/8\pi R_B C_{CB})^{1/2}$. No noticeable change in R_B was observed with the dose variation. It is also noted that the collector current at peak f_T is lowered with reduced SIC dose (Fig. 6), owing to the accelerated onset of the Kirk Effect.

SIC dose variation also affects the avalanche breakdown behavior of bipolar transistors as the electric field in B-C SCR is modulated. The multiplication factor $M - 1$, extracted from the V_{CB}-dependence of I_C with a forced I_E of 10 μA (see inset of Fig. 7), is illustrated in Fig. 7 as a function of V_{CB} for the three SIC conditions. It clearly shows the suppressed level of the avalanche multiplication in B-C SCR with the reduced SIC dose, owing to the diminished electric field inside. The reduced $M - 1$ leads to an increase in the breakdown voltages, as summarized in Table 1 along with $M - 1$ values at $V_{CB} = 2$ V.

In conclusion, it is observed that the SIC dose variation affects f_T and f_{max} in opposite directions in 300 GHz SiGe HBTs, which can be exploited to selectively optimize the devices for either f_T or f_{max}, depending on the requirement from a given application. This trend also indicates, along with the observed SIC dose dependence of the breakdown voltages, that the traditional speed-breakdown voltage (BV) tradeoff is valid for f_T-BV, but not necessarily for f_{max}-BV.

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[1] J. –S. Rieh et al, *IEDM Tech. Dig,* p. 771, (2002). [2] B. Jagannathan et al, *EDL* 23(5), p. 258 (2002).

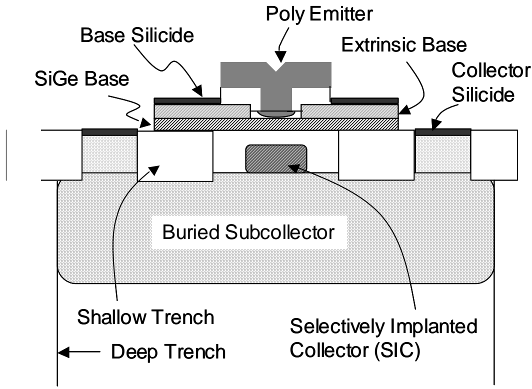


Fig. 1: Schematic cross section of the SiGe HBT.

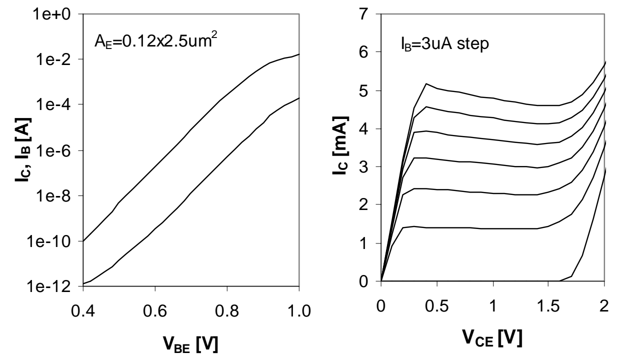


Fig. 2: DC characteristics of control device (SIC_H).

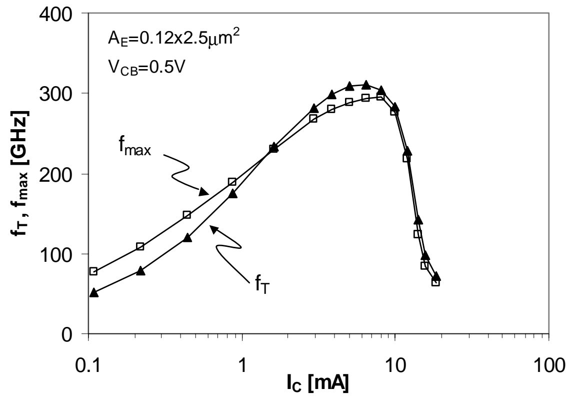


Fig. 3: RF characteristics of control device (SIC_H). Peak f_T and f_{max} are 310 GHz and 295 GHz, respectively.

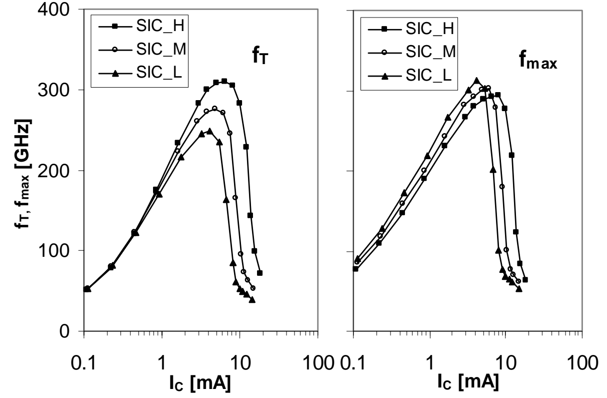
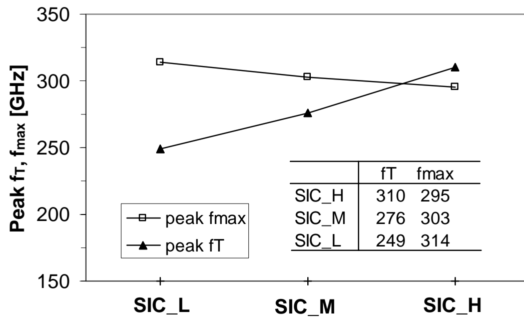


Fig. 4: Effect of SIC dose variation on f_T and f_{max}. Reduced dose leads to increased f_{max} and decreased f_T.



	fT	fmax
SIC_H	310	295
SIC_M	276	303
SIC_L	249	314

Fig. 5: Trend of peak values of f_T and f_{max} with various SIC conditions.

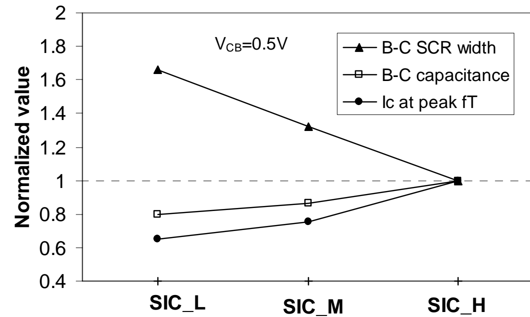


Fig. 6: Trend of B-C space charge region width, B-C capacitance (C_{CB}), and collector current (I_C) at peak f_T with various SIC conditions (all values normalized to SIC_H case).

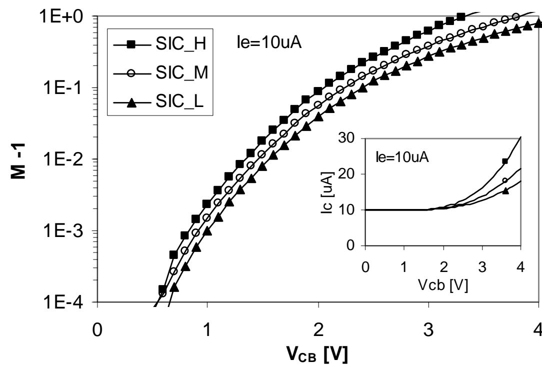


Fig. 7: Multiplication factor M – 1 for various SIC conditions. Inset shows I_C with forced I_E of 10 μA, from which M – 1 values were extracted.

Table 1: Selected avalanche breakdown parameters. M – 1 is obtained at V_{CB} = 2 V.

	M – 1 (2V)	BV_{CBO}	BV_{CEO}
SIC_H	0.087	5.4 V	1.6 V
SIC_M	0.055	6.2 V	1.7 V
SIC_L	0.035	6.7 V	1.8 V